CADSTAR

CADSTAR Signal Integrity Verify

D A T A S H E E T

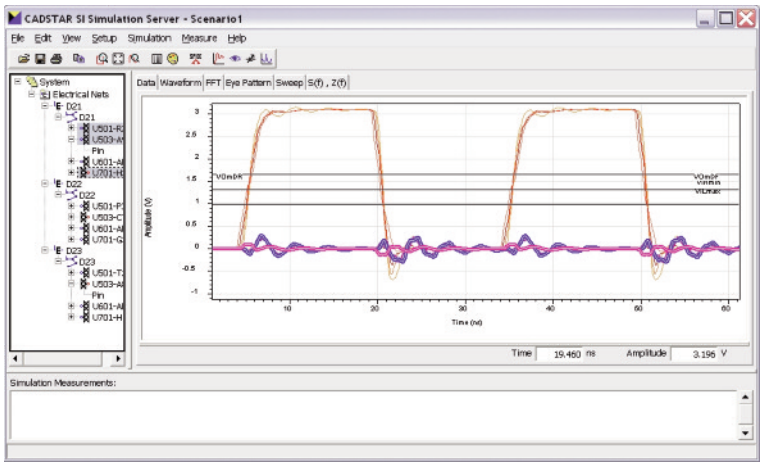
BENEFITS

- complete post-layout signal integrity simulation toolset
- seamlessly integrated with CADSTAR Design Editor
- simulation of ‘what if’ scenarios
- fast calculation of reflection and cross talks effects
- evaluation of effects of proposed layer stack changes, track widths or track to track speeding

According to industry experts, mainly due to the fast edge rates of modern ICs, over 80% of today's multi-layer PCB designs are high-speed, needing special design strategies to ensure design quality, data integrity and successful operation. This trend is set to continue with the introduction of new IC technologies, new interconnect strategies like high speed serial, increased board density, growing importance of programmable devices like FPGAs, and shorter development cycles. To operate as desired, designs must fulfill many complex and often contradictory signal quality and timing demands. Working to old 'rules of thumb' will no longer be adequate to meet these requirements; to be successful, you need new tools with simulation capabilities.

CADSTAR SI Verify is a CADSTAR solution that offers a complete post-layout signal integrity simulation toolset, seamlessly integrated into CADSTAR Design Editor. It uses an accurate transmission line simulation approach to analyze reflection and crosstalk effects, and to calculate the relevant timing information and delays.

The required electrical parameters of transmission lines (phase velocity, inductance and capacitance matrices, characteristic impedances) are determined by a 2D field solver using boundary element or finite element methods. The time domain signal integrity simulation offers a fast calculation of reflection and crosstalk effects on printed circuit boards, considering also the non-linear characteristics like clamping.



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Product Information

CADSTAR SI Verify consists of four main components:
-Design Verification Management
-'What-If' Analysis
-Layer Stack Definition
-Simulation
All four use and share the same single EMC Device Library.

Design Navigation

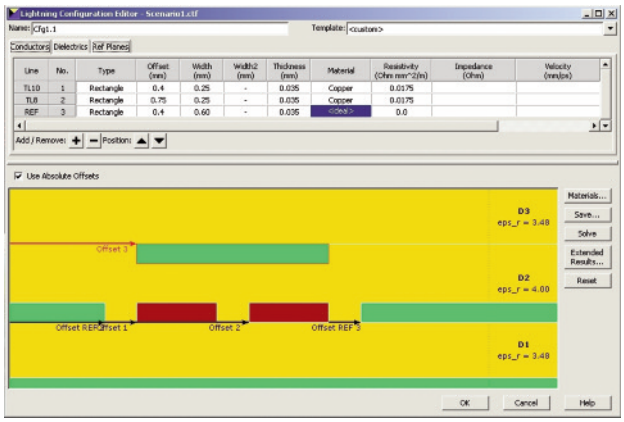
The spreadsheet based Constraint Manager of CADSTAR SI Verify enables hierarchical design navigation and verification of design constraints against the physical implementation using interactive simulation on a per net base or batch simulation for any selected number of nets of the PCB.

'What-If' Analysis and Pre-Design SI Studies

A graphical so called Scenario Editor provides a 'what-if' scratchpad, allowing you to experiment with different design strategies. Equivalent circuits are automatically generated from the physical layout, and various options, e.g. on terminations or topologies, can be verified through simulation.

Layer Stack Definition

You can interactively define and modify the layer stack / track cross-sections to drive the field solver. Determination of the characteristic impedance of transmission lines, modification of the conductor and dielectric cross-sections, as well as the impact of using different materials, is also possible. You can extract cross-sections from the physical design, and save your own arrangements as templates. Thus you can evaluate the effects of proposed layer stack changes, different track widths, and track-to-track spacing. Freqeuncy dependend losses are taken into account for accurate simulations in the GHz area.



EMC Device Library

The EMC Device Library of SIV is used to add and edit behavioral IC models.

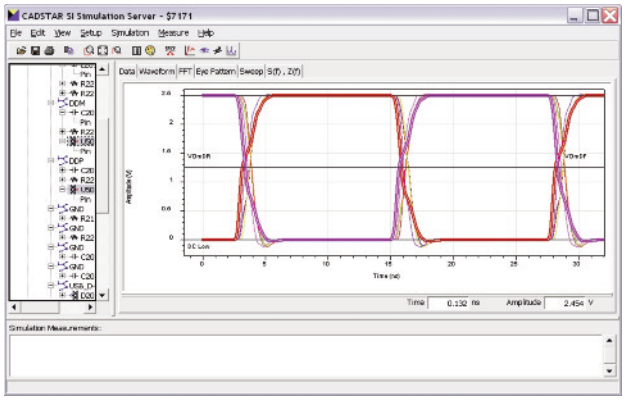
You can import IBIS (see http://www.eigroup.org/ibis/ibis.htm) standard device models, and check or modify their behavior and quality graphically, or easily define your own models for ICs, passive devices or various connector types. You can also map to device models in your master library, or use simple mouse click model assignment in the design navigation cockpit.

Passive SPICE models can be used as well, i.e. to model EMC filters, and equivalent circuit models which the user can create are capable to model any kind of passive parasitic.

Interactive / Batch Simulation

CADSTAR SI Verify gives you the option of interactive and batch simulation to derive voltage or current versus time. On a single mouse click it is possible to obtain frequency domain results like S-Parameter or transmission line impedance versus frequency and you can view results as a Fast Fourier Transformation or Eye Diagram too.

There is no need to define separate models, and an identical user interface throughout the verification process is provided. You can simulate the both physical design, including multiple variants, and 'What-If' scenarios. Differential pairs are simulated as single electrical entities.



Coupled Transmission Lines

Interactive reflection and crosstalk simulation results are displayed in a new simulation control window, with measurement and result export facilities.

Parameter Sweep

The parameter sweep feature allows you to experiment with values of passive devices or lengths of transmission lines in order to determine the optimal values according to the design requirements. A representation of all waveforms can be exported to Windows Clipboard, to XML or outputs such as CSV, enabling checks in MS-Excel or other tools and allowing a documentation of the simulation work.

At the Cutting Edge

High-speed design is a rapidly evolving field, and with CADSTAR SI Verify you can be sure of having the features to keep you at the forefront. Latest developments include:

-Waveforms at Die

  -Accurate timing and waveform measurements possible at ICDie level, helping choose the best IC packaging for your design.

-Trapezoidal trace field solution

  -Improves precision of characteristic impedance calculations in scenarios to cover the under-etching manufacturing tolerances from the PCB design process.

-RF via and passive equivalent circuit models

  -How lead and trace parasitics affect your choice of decoupling capacitors and how, in detail, vias may affect very high speedcircuits.

-Simultaneous current and voltage waveform views

  -Check transient demand on power supplies while evaluating signal quality.

-Improved Electrical Board Description (EBD) handling

  -Check signal integrity and real interconnect timing for complete analysis of motherboard/daughterboard (multiboard) set-ups.

More

CADSTAR is a fully featured PCB Design System renown for its excellent price-performance ratio. From simple single-sided through-hole designs to multi-layer, surface mount, high-speed digital and analogue designs, CADSTAR is capable of designing today's most demanding Printed Circuit Boards. From schematics, board- and FPGA level system design, PCB layout, high-speed and signal integrity, analysis, 3D, creation of manufacturing output, to complete data management capabilities and extensive internet-accessible libraries containing over 200,000 components, CADSTAR provides you with all technologies necessary for a complete electronic development process in one environment.

For more information on all the tools and solutions available with CADSTAR, please visit www.zuken.com/CADSTAR

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